Si3482 Smart PSE-24 Kit User's Guide

1. Introduction

The Si3482 power management controller works with Si3452 PSE controllers and enables the use of a smaller, lower-cost, and more efficiently-utilized power supplies in managed or unmanaged Power over Ethernet (PoE) Power Sourcing Equipment (PSE) with up to 48 ports and up to three parallel power supplies. The Smart PSE-24 kit demonstrates the use of the Si3482 in a 24-port system. Figure 1 shows the assembled kit.

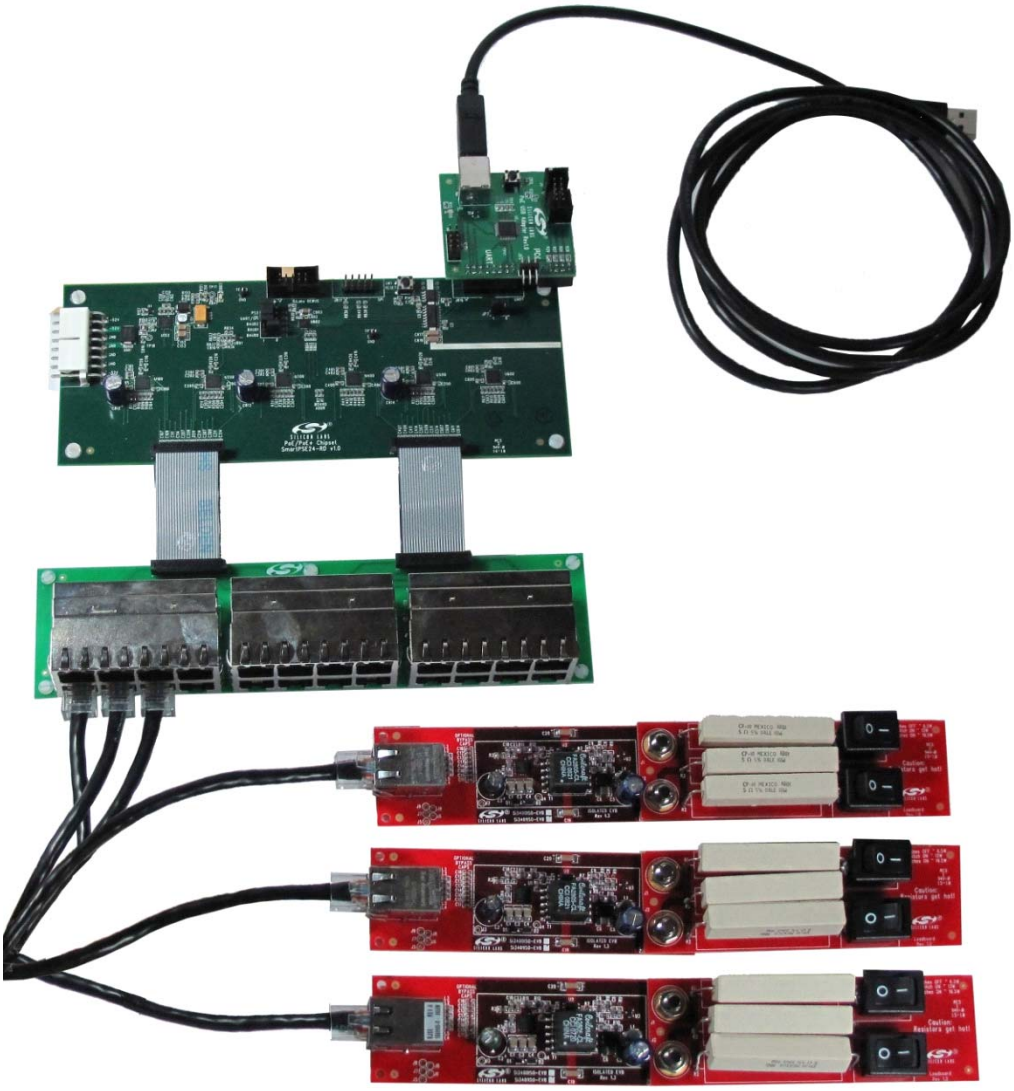


Figure 1. Smart PSE-24 Kit

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2. Smart PSE-24 Kit Contents

Table 1 lists the contents of the PSE-24 kit.

Table 1. PSE-24 Kit Contents

1	The SmartPSE24-RD, which includes the Si3482, six Si3452 PoE controllers, a –50 V to +3.3 V dc-to-dc converter based on a Si3500, isolation for UART communications, and an alternative SPI interface (the SPI interface is not isolated).
2	Two Si3402ISO-EVB powered device evaluation boards. The boards are configured to provide a Class 3 signature.
3	One Si3402ISO-C4- EVB. This board is configured to supply a Class 4 signature. The Class 4 boards are marked Class 4 and can also be identified by the diodes on the back of the board.
4	Three switchable loads. The switchable loads draw approximately 6.5, 13, or 19.5 W from the PSE.
5	One 24-port connector board to bring the Si3452 power to Ethernet jacks. The connector board does not have Ethernet data functionality.
6	PoE USB adapter. This adapter supports USB to UART, SPI or I^2C. It is generally used for UART with the Smart PSE 24 Kit.
7	Three Ethernet cables, one USB cable, and two 24-wire ribbon cables.

3. Using the Smart PSE-24 Kit

3.1. Hardware Configuration

The boards are connected as shown in Figure 1. A nominal 50 V power supply is connected to J815 (note the polarity). For high-power support according to the IEEE standard, the supply voltage should be between 51 and 57 V. For normal power levels, the power supply can be 45 to 57 V. The total power supply wattage can be as high as 720 W for full power on all ports. Effective evaluation can be done with a power supply of 40 W or more. Once configured, the Si3482 manages the available power.

The large diode, D801, will be forward-biased in case of incorrect input polarity.

Note: It is recommended that the power supply be connected to the board and then turned on so as to reduce large inrush current charging the (3) 33 µF filter capacitors on the board.

Table 2 lists the jumper settings.

Table 2. Jumper Settings

Jumper	Logic Level	Reason
JP7	1	Si3482 is not reset when the PoE USB adapter is removed.
JP8	1	JP8 selects UART or SPI interface. The PoE USB adapter board is generally set for UART.
JP4, JP5, JP6	1,1,1	JP4, JP5, and JP6 set the UART baud rate. The PoE USB adapter is configured for 115.2 kHz
JP9	0	JP 9 is for testing the power supply removal function for the third power supply. As will be discussed later, the power manager GUI can control the first and second power supply lines. The status of the third power supply line is reported but cannot be controlled. Generally, JP9 is set to 0 (power supply 3 not inserted).

3.2. Installing the PoE USB Adapter

Note: Before the PoE USB adapter is plugged in, the device driver should be installed.

To install the PoE USB adapter drivers, run PoEUSBSetup.exe from the supplied disk, and follow the instructions including accepting the end user license agreement. The PoE USB adapter supplied with the Smart PSE-24 Kit has been tested to be compatible with Windows XP®, Windows Vista®, and Windows 7® operating systems.

After successful installation, plug in the USB cable; the PoE USB device should be recognized. For Windows XP, select “No not at this time” when Windows prompts to search for software, and select “Install the software automatically” on the next screen. After successful installation, a PC reboot may be required.

4. Demonstration Use of the Power Manager GUI

The Silicon Labs power manager GUI is used to configure and observe the Smart PSE 24 via the supplied PoE USB adapter. See the Si3452 Power Management GUI user’s guide for detailed installation instructions. Note that once the Si3482 has been configured, it can run in hardware only mode without the GUI or PoE USB-to-UART adapter.

The demonstration assumes the Power Manager GUI has been used to configure the Si3482 as follows:

- 40 W of power available on Power Supply 2. Set Power Supply 1 to zero for demonstration in the standalone mode. This is because, in the standalone mode, the control line for Power Supply 1 status is low (disabled) when the USB cable is unplugged.
- Port 1 High Power (PoE+, 30 W) all other ports standard PoE (15.4 W)
- Port 1 critical priority; all other ports low priority
- Consumption-based power management
- Retry after reconnect for overloads

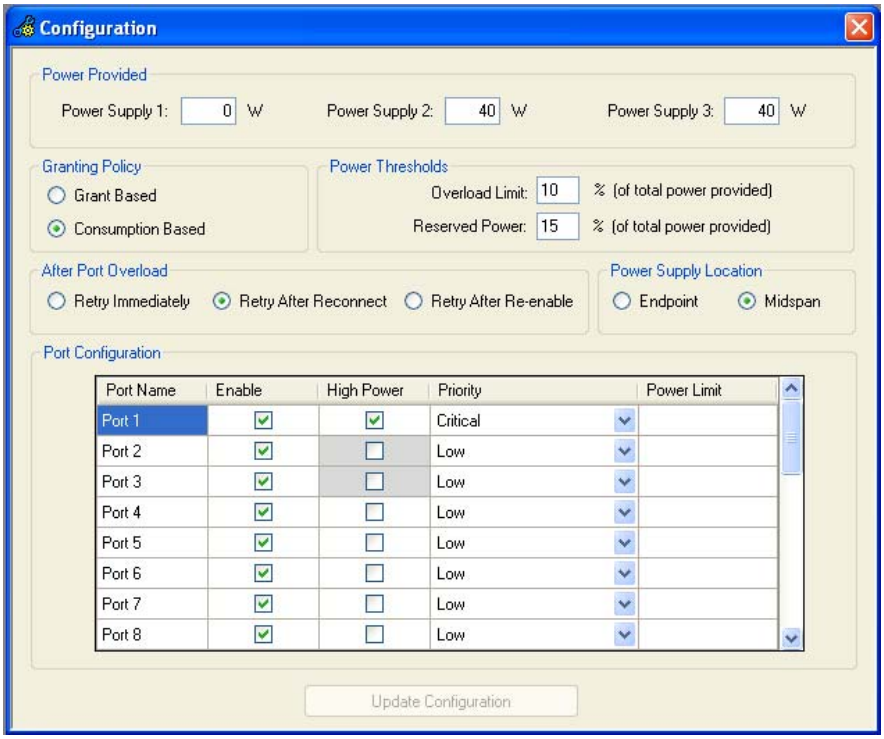


Figure 2. Configuration Screen

- Power Supply 2 inserted. Power Supply 1 can be inserted or not as its power capacity is set to zero. Power Supply 3 should also display as not inserted if JP 9 is set low. Power Supply 3 cannot be controlled by the GUI when using the Smart PSE 24 Kit because jumper JP9 sets the status.

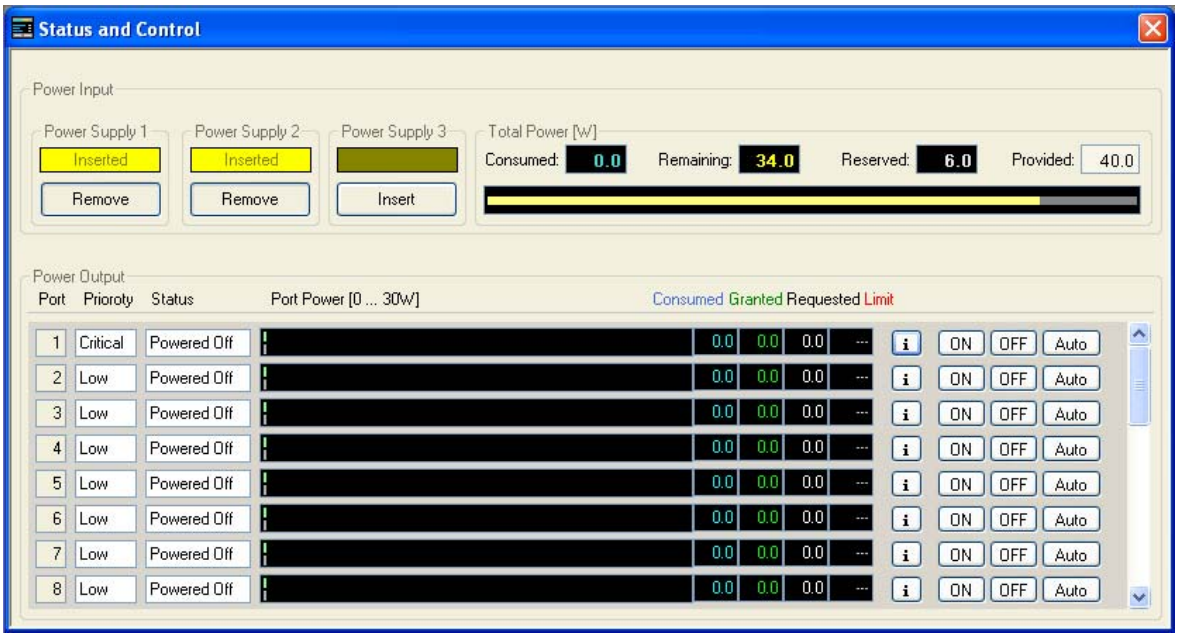


Figure 3. Initial Status Screen

The Si3482 Smart Power 24 kit ships with three powered devices based on the Si3402 with loads for up to approximately 19.5 W of input power. The loads are arranged as one to three 5 Ω resistors, which draw 5 W each at the PD output voltage of 5 V. Due to the PD input diode bridge and the dc-to-dc conversion efficiency, each resistor causes approximately 6.5 W of power to be drawn from the PSE. This means that the PD will draw approximately 6.5, 13, or 19.5 W from the PSE, depending on the number of load resistors connected.

Step 1: Connect a Class 3 PD with a 6.5 W load (switches off) into Port 1 and a Class 4 PD with a 6.5 W load into Port 2.

The status window is shown in Figure 4.

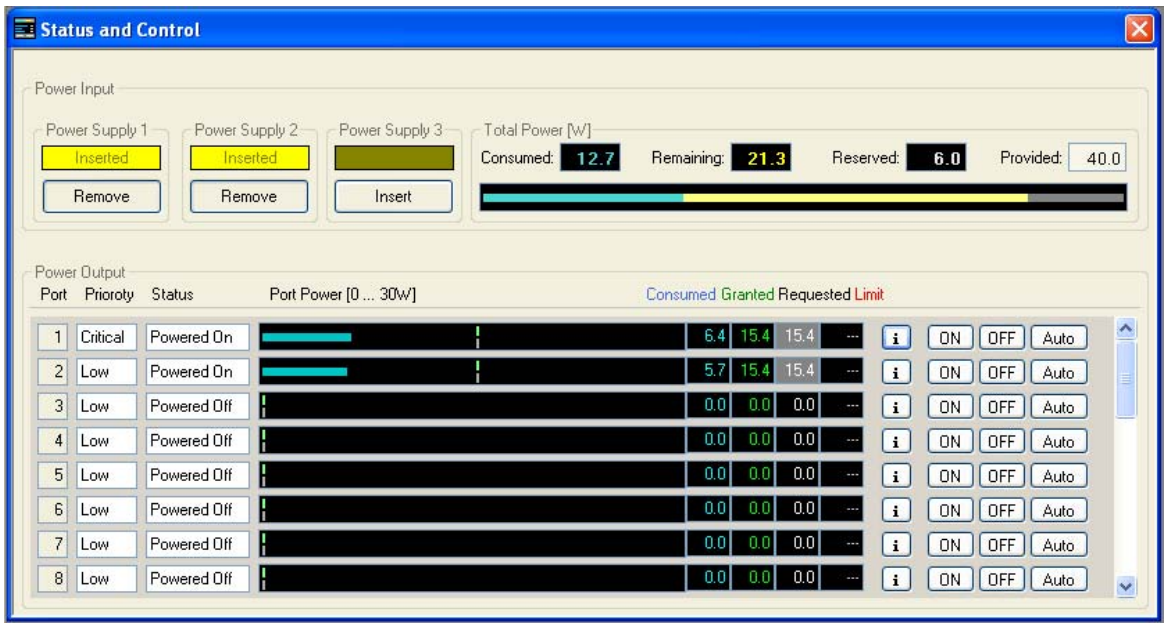


Figure 4. Status Screen with Class 3 PD on Port 1 and Class 4 PD on Port 2

Since sufficient power is available, both ports are granted power. Because Port 2 was not enabled as PoE+, the Class 4 PD is only granted 15.4 W.

Step 2: Disconnect the PDs from Step 1, and connect the Class 4 PD to Port 1 and Class 3 PDs to each of Ports 2 and 3. Initially, use a 6.5 W load on each PD.

All three ports are granted power. Port 1 is now granted 30 W since Port 1 is enabled for high power (PoE+). Since only one resistor is connected, approximately 6.5 W is drawn on each port.

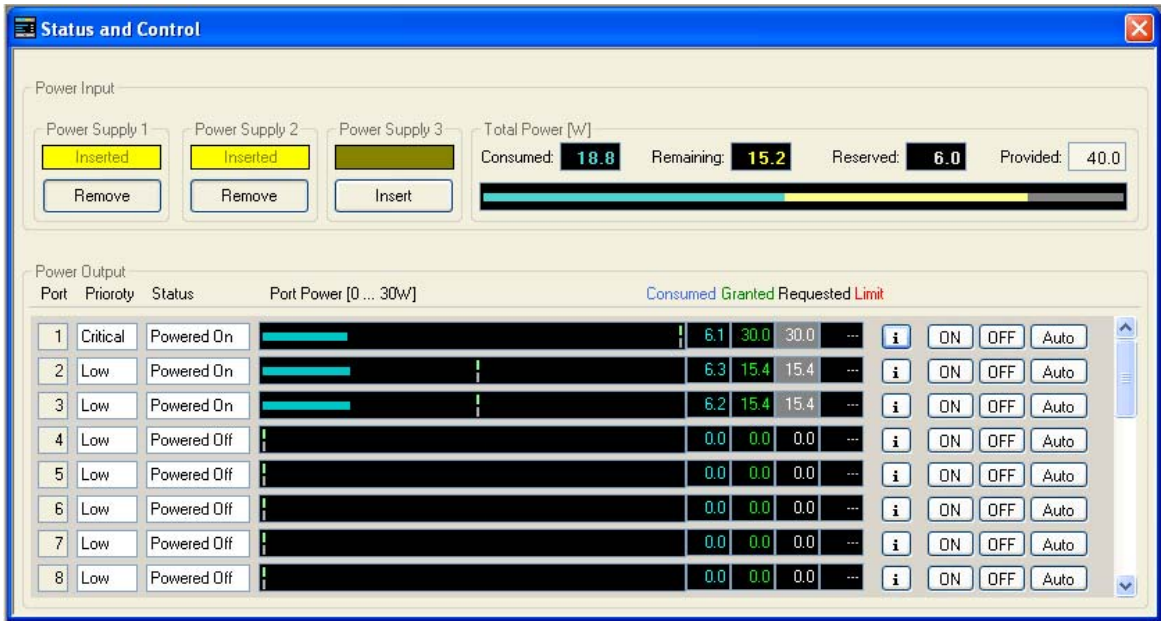


Figure 5. Status Screen with Class 4 PD on Port 1 and Class 3 PDs on Ports 2 and 3

Step 3: Increase the Load on the ports to create a port overload by switching in more load resistors.

For Port 2 or Port 3 (with Class 3 PDs), the port overload condition occurs with the three resistors, which corresponds to about 19.5 W of input power. The following screen shot shows the result of an overload (indicated by the status “blocked”) on Port 3.

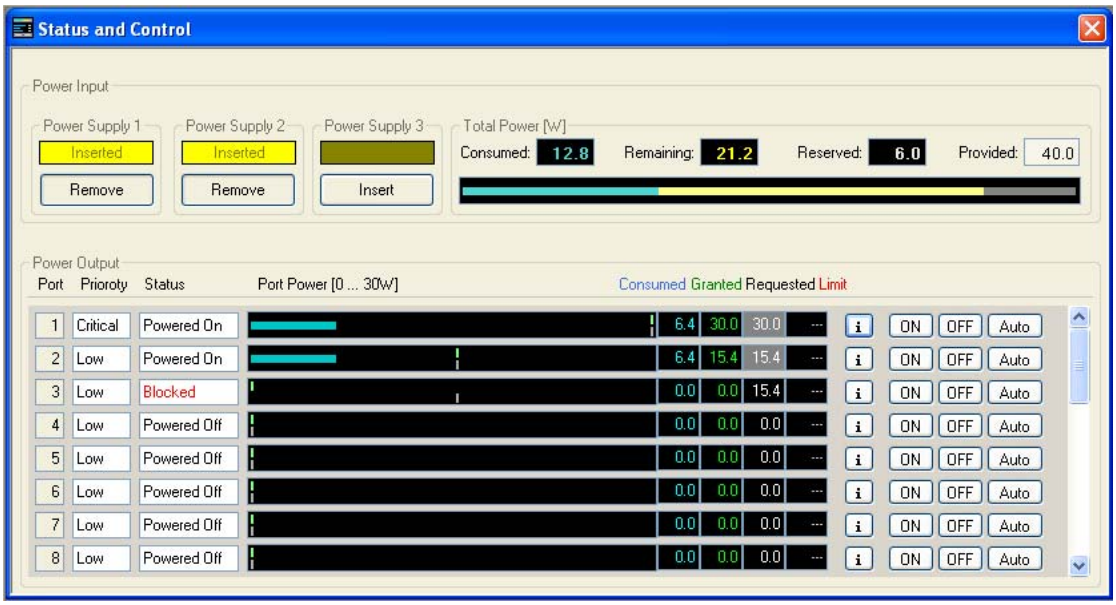


Figure 6. Status Screen after an Overload on Port 3

To reset the port, decrease the load back to one resistor; unplug the PD, and plug it back in. This demonstrates “retry after reconnect”.

For Port 1 (PoE+ port with Class 4 PD), the overload does not happen even with 19.5 W being drawn by the PD.

Note: Use caution because, in this case, the load resistors and PD will get hot.

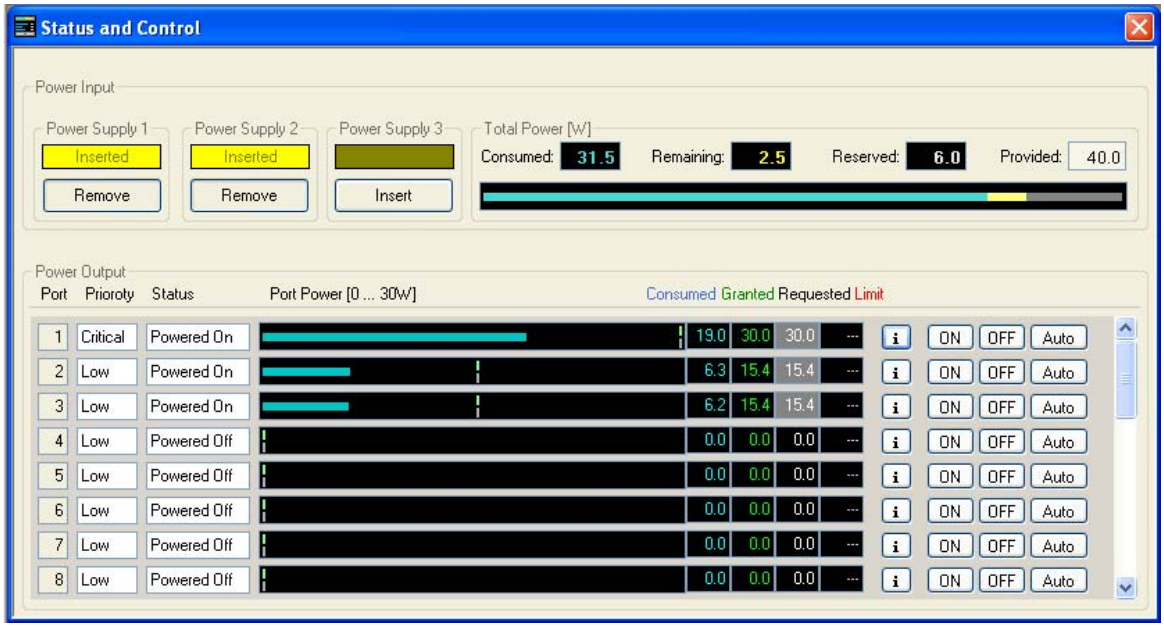


Figure 7. Status Screen Showing Class 4 PD on Port 1 Drawing 19 W

Step 4: Demonstrate the port priority and system overload protection features.

Disconnect all PDs, and then connect the Class 3 PDs to Ports 2 and 3 with two load resistors so that they draw 13 W each (26 W total power).

Connect the Class 4 PD with three resistors (19.5 W) to Port 1. Port 1 is granted power, and a system-level overload is created with approximately 45.5 W. Either Port 3 or Ports 2 and 3 will be turned off depending on whether the Si3480 reported a severe overload (>44 W). Because the PDs have a soft start circuit, it is possible that only Port 3 is turned off when the power exceeds 40 W. The ports that are turned off will not turn back on until the load on Port 1 is reduced. This is because there is not enough power available to grant 15.4 W from the Class 3 PD.

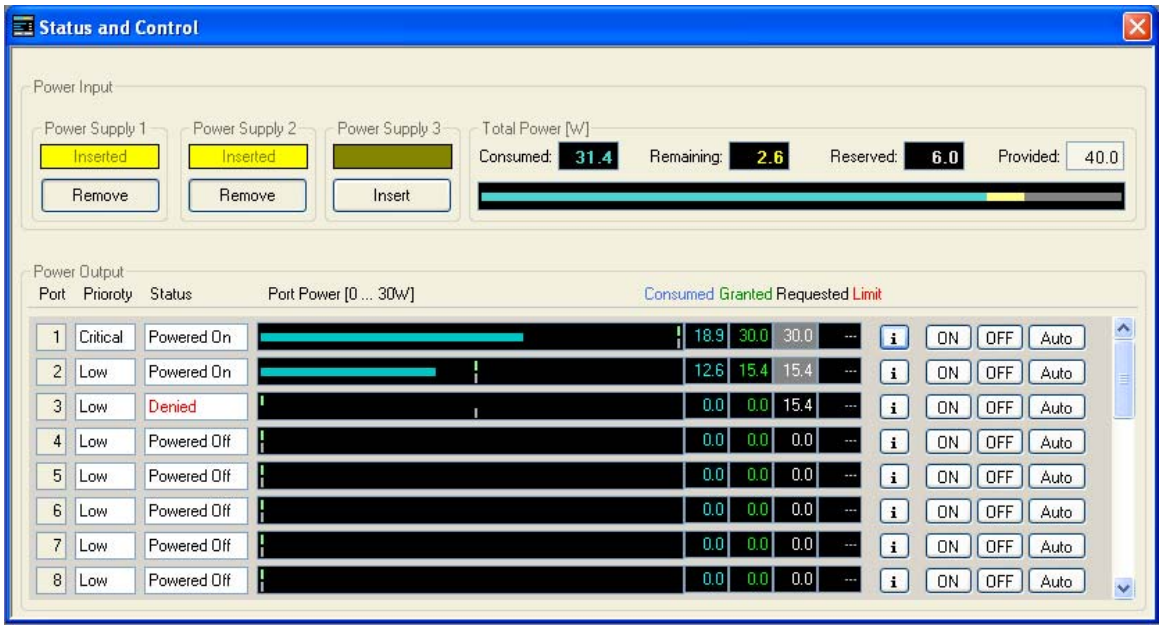


Figure 8. Status Screen Showing Port 3 Denied Power Due to Insufficient Power Available

The Si3482 will manage power on all Si3452 devices to which it is connected. The number of Si3452 devices connected is discovered upon power up. This means that the Si3482 can manage power on up to 48 ports.

Once configured, the Si3482 will continue to manage the power even when the host is disconnected. To demonstrate this, exit the GUI, disconnect the PoE USB adapter, and repeat the above tests. While there is no visual display, the behavior is the same. The PD status can be seen by looking at the LEDs on the Si3402 evaluation boards located on the RJ-45 connector. These LEDs glow steadily if power is supplied.

Note that, in the schematics shown in Figure 6, the Reset and Pgood2 signals are routed through an Si8423 isolator. The Si8423 default state is high so that, when the USB connector is removed, the Si3482 is not held in reset, and Power Supply 2 is still configured as inserted. This is why Power Supply 2 was chosen to be inserted in the above examples.

4.1. Easing Software Development with the Serial Packet Protocol SDK

A host MCU uses the Serial Packet Protocol (SPP) to communicate with an Si3482 Power Management Controller. A Serial Packet Client in the host MCU implements the client side of the Serial Packet Protocol. The SPP Software Development Kit (SDK) provides the source code for the Serial Packet Client, greatly reducing the software development effort needed to use an Si3482.

The software included with this SMARTPSE24-KIT includes the SPP SDK and related documentation. Please refer to that software as well as the Si3482 data sheet for further details on taking the next step in development with the Si3482 power management controller.

4.2. Schematics

The following figures show the detailed schematics, BOM, and layout for the Si3482evaluation board.

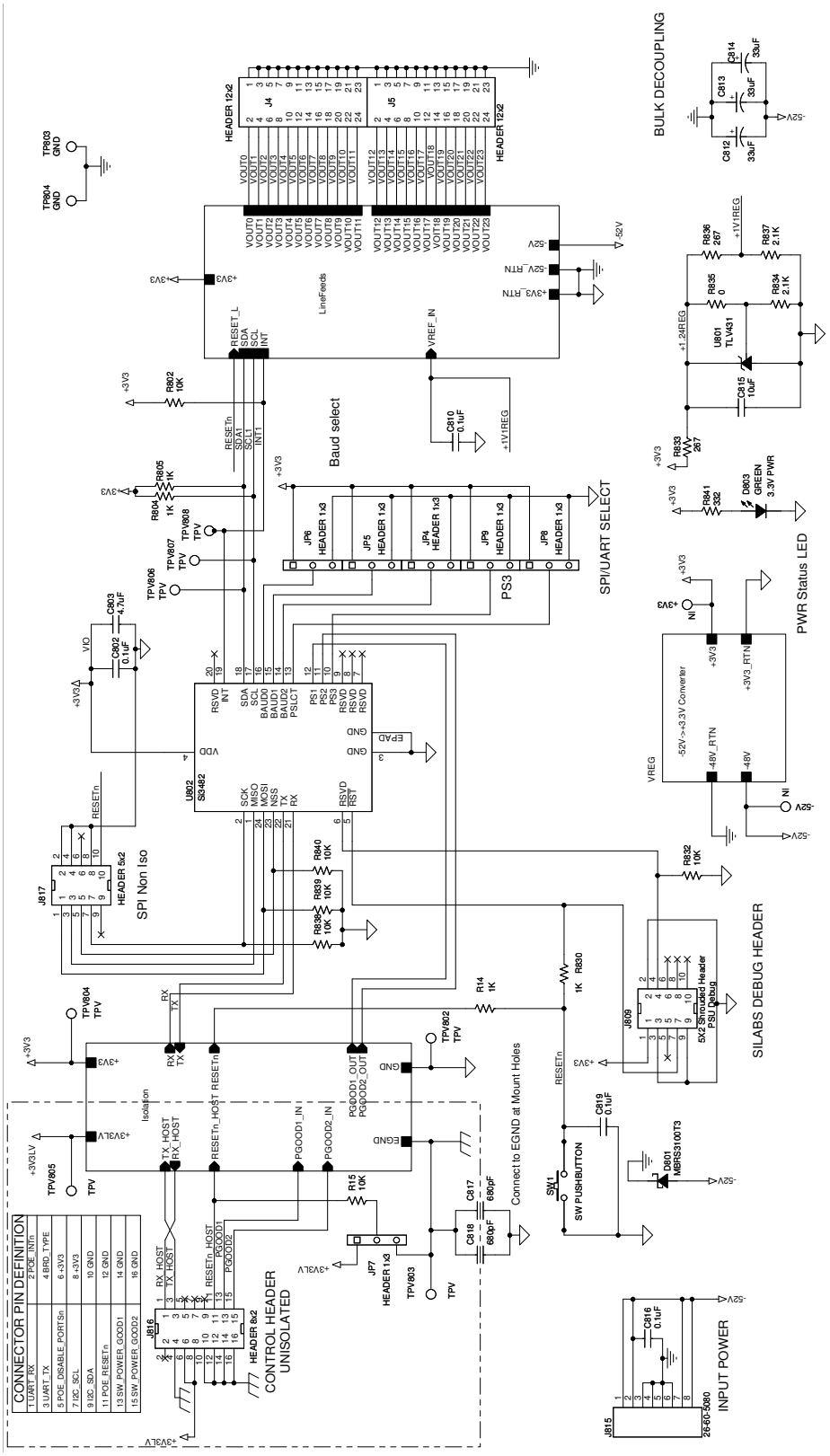


Figure 9. Si3482 power manager and top level board schematic

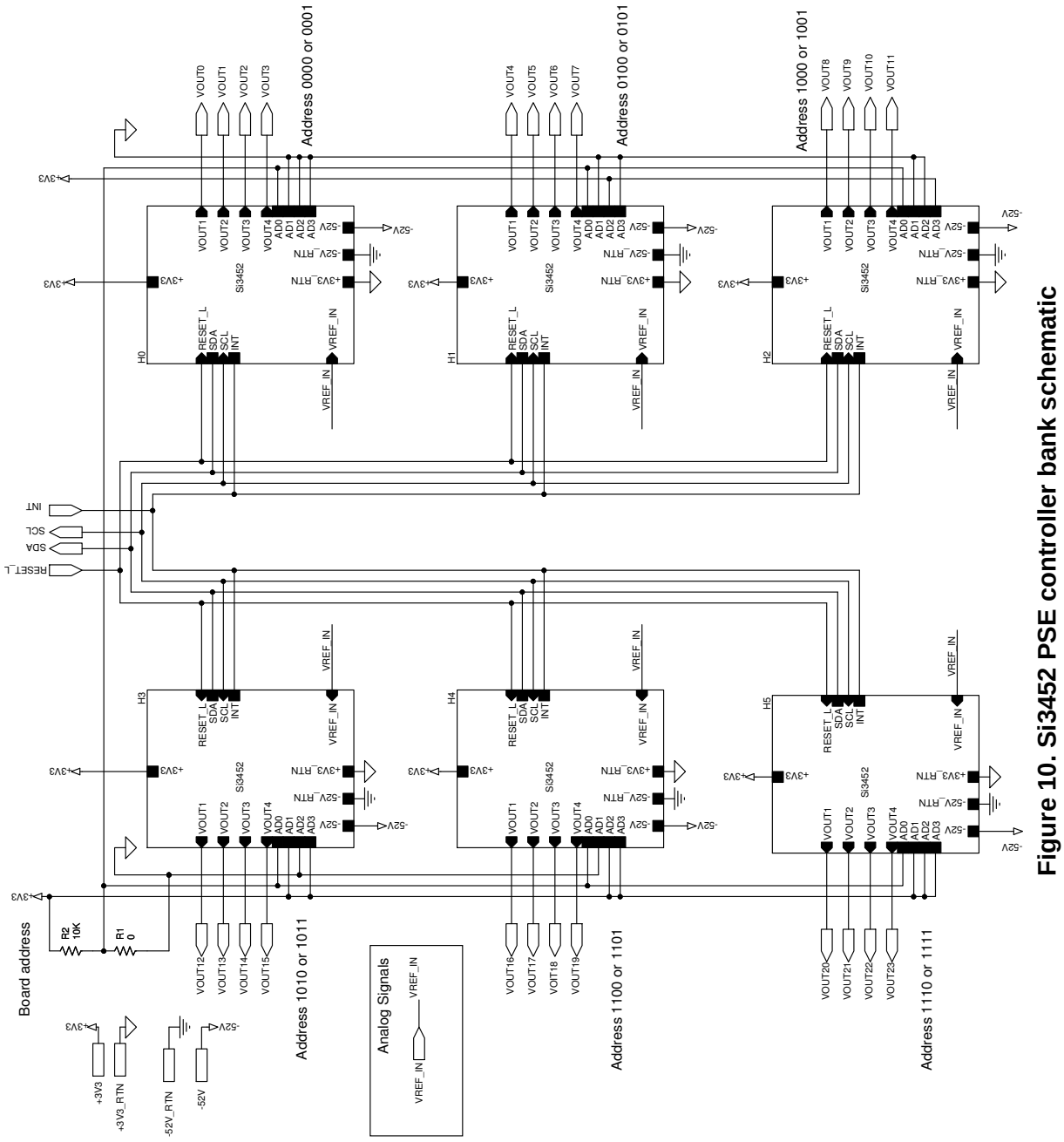


Figure 10. Si3452 PSE controller bank schematic

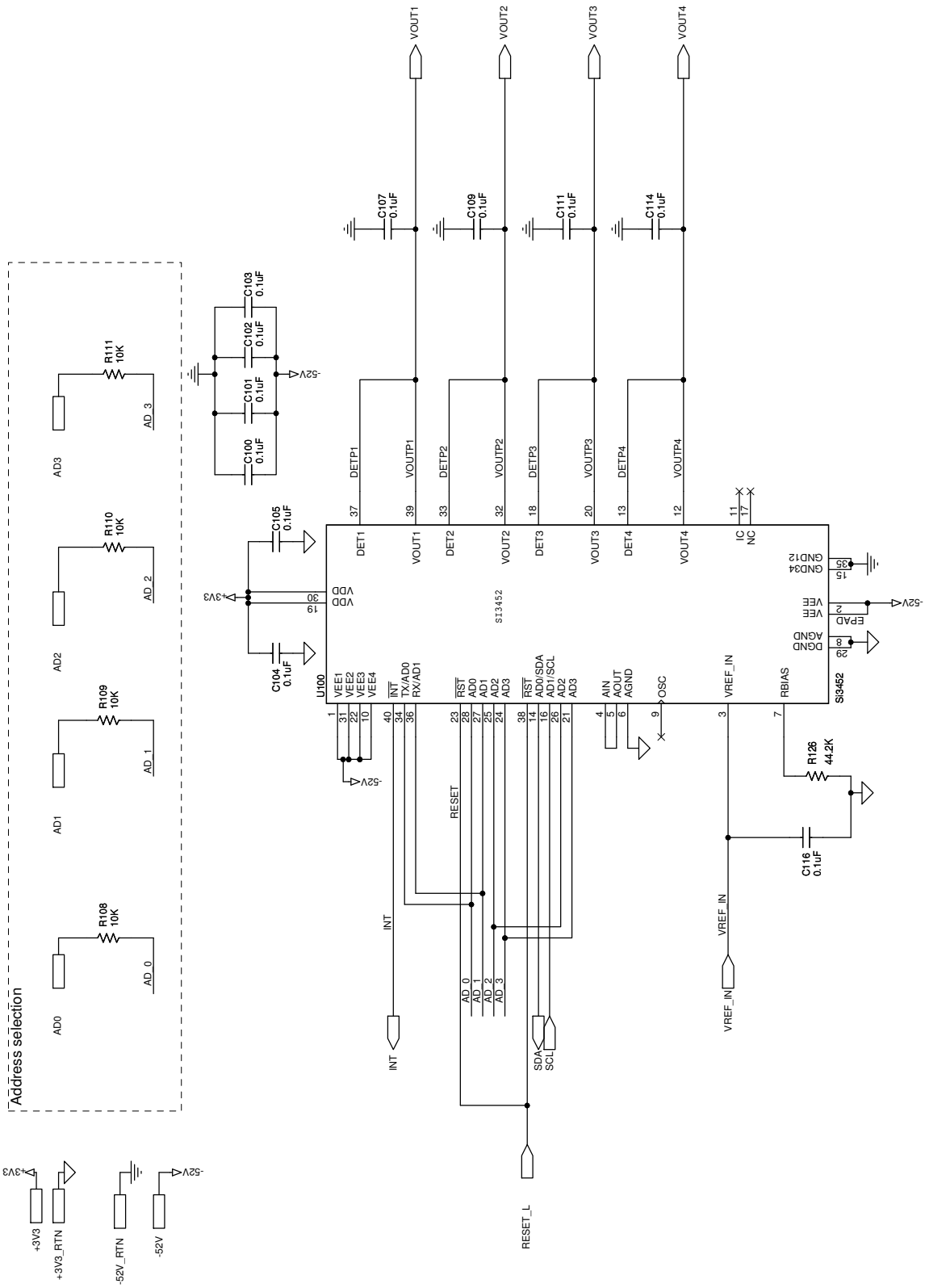


Figure 11. Si3452 PSE Schematic Detail

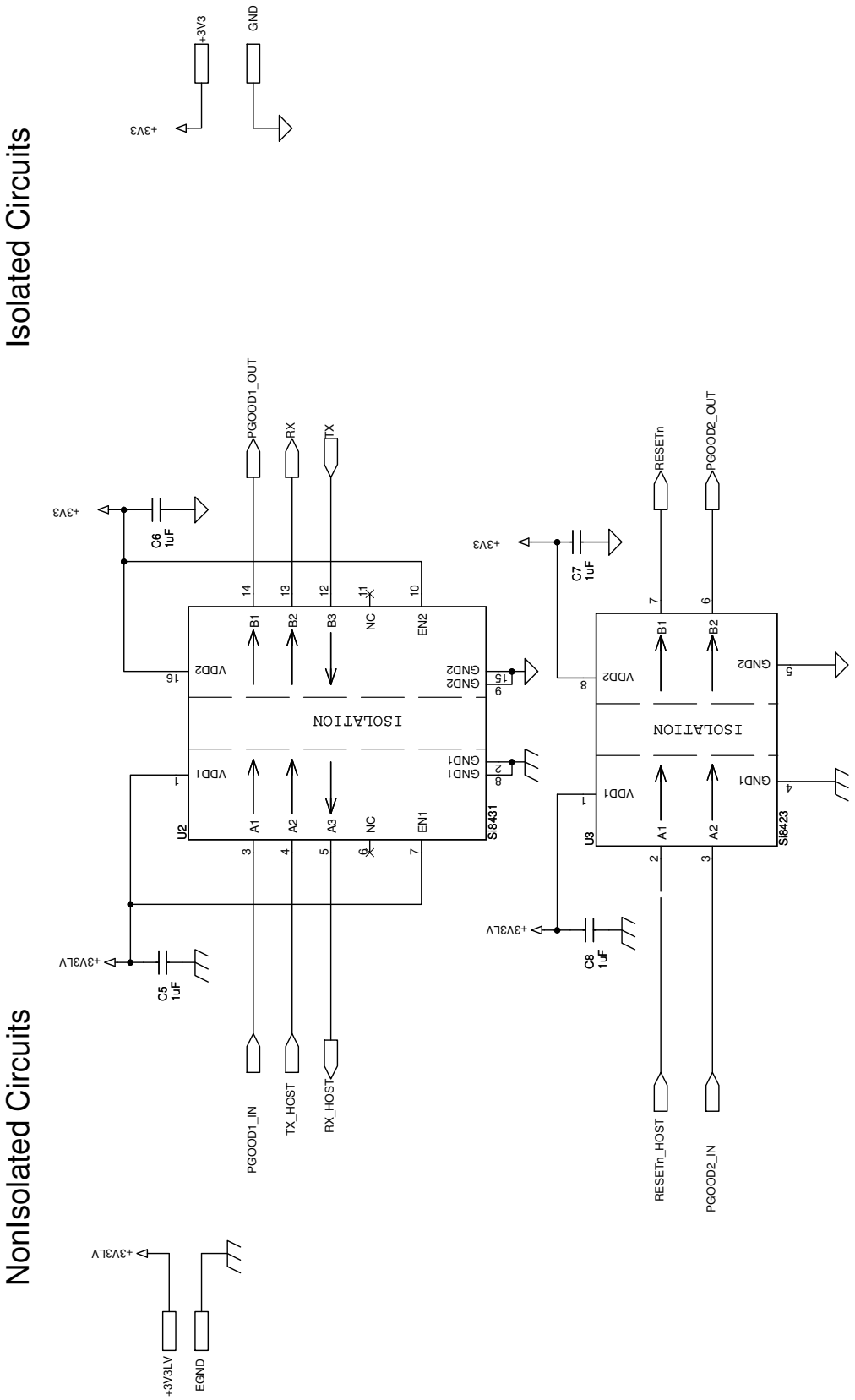


Figure 12. UART Isolator Circuitry

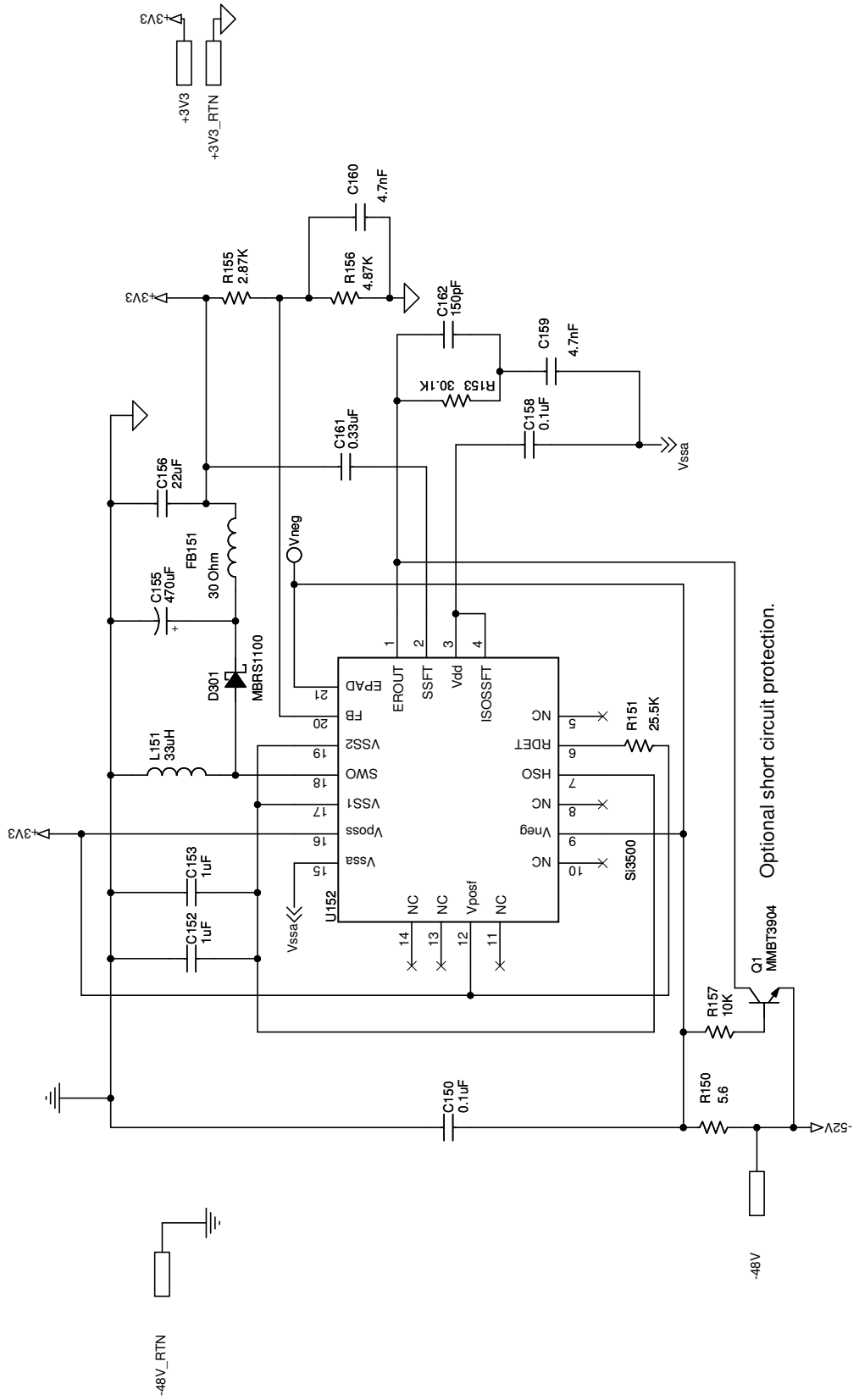


Figure 13. DC to DC converter

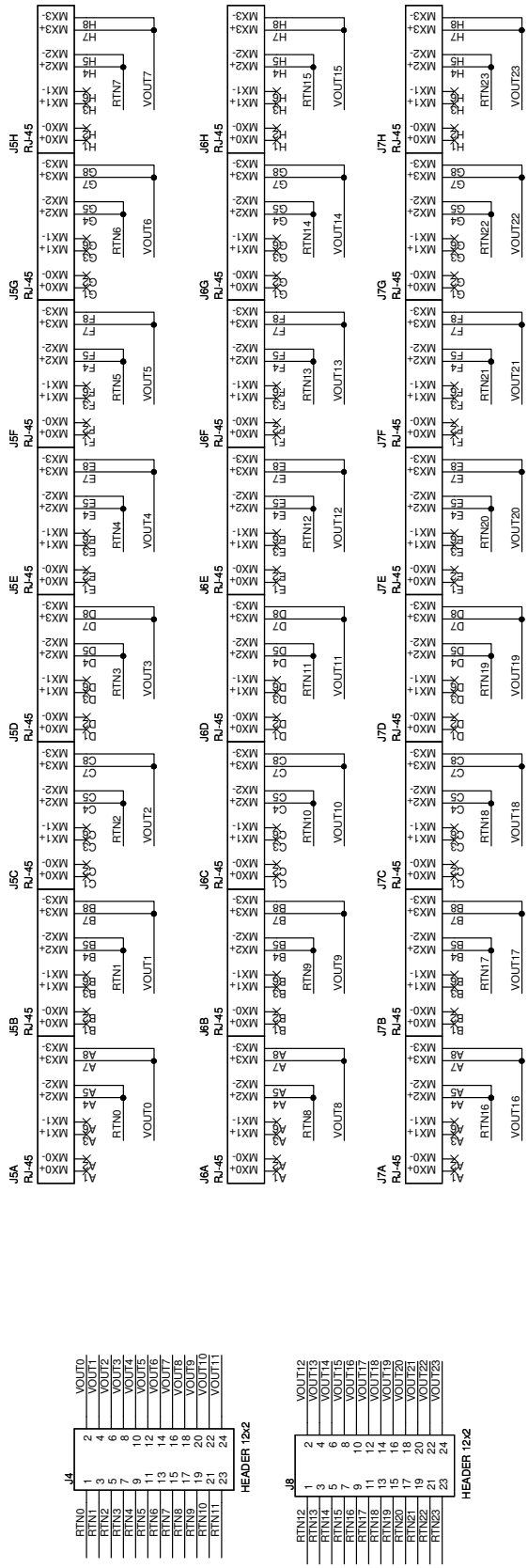


Figure 14. RJ-45 Ethernet Cable Connector Board

4.3. Bill of Materials

Table 3. Si3482 Smart PSE-24 Bill of Materials

Item	Qty	Ref	Value	Rating	Tol	PCB Footprint	Mfr Part #	Mfr
1	4	C5,C6,C7,C8	1 µF		±20%	C0805	C0805X7R160-105M	Venkel
2	50	C100,C101,C102, C103,C107,C109, C111,C114,C150, C200,C201,C202, C203,C207,C209, C211,C214,C300, C301,C302,C303, C307,C309,C311, C314,C400,C401, C402,C403,C407, C409,C411,C414, C500,C501,C502, C503,C507,C509, C511,C514,C600, C601,C602,C603, C607,C609,C611, C614,C816	0.1 µF		±20%	C0603	C0603X7R101-104M	Venkel
3	20	C104,C105,C116, C204,C205,C216, C304,C305,C316, C404,C405,C416, C504,C505,C516, C604,C605,C616, C802,C810	0.1 µF		±20%	C0603	C0603X7R160-104M	Venkel
4	2	C152,C153	1 µF		±10%	C1210	C1210X7R101-105K	Venkel
5	1	C155	470 µF	45 mΩ ESR	±20%	C7343D	T495D477M006ATE0457280	Kemet
6	1	C156	22v		±20%	C0805	C0805X5R6R3-226M	Venkel
7	1	C158	0.1 µF		±10%	C0603	C0603X7R250-104K	Venkel
8	2	C159,C160	4.7 nF		±10%	C0603	C0603X7R160-472K	Venkel
9	1	C161	0.33 µF		±10%	C0603	C0603X7R100-334K	Venkel
10	1	C162	150 pF		±10%	C0603	C0603X7R160-151K	Venkel
11	1	C803	4.7 µF		±20%	C1206	C1206X7R100-475M	Venkel
12	3	C812,C813,C814	33 µF		±20%	C3.5X8MM-RAD	ECA2AM330	Panasonic
13	1	C815	10 µF		±20%	C0603	C0603X5R6R3-106M	Venkel
14	2	C817,C818	680 pF	Y3	±15%	C1808	GA342QR7GD681KW01L	MuRata
15	1	C819	0.1 µF		±20%	C0805	C0805X7R160-104M	Venkel
16	1	D301	MBRS1100	1 A		DO-214AA	MBRS1100T3	On Semi
17	1	D801	MBRS3100T3	3 A		DO-214AB	MBRS3100T3	On Semi
18	1	D803	GREEN	30 mA		LED-0805-K	LTST-C170GKT	Lite_In Inc
19	1	FB151	30 Ω	1000 mA		L0603	BLM18PG300SN1	MuRata
20	6	JP4,JP5,JP6, JP7,JP8,JP9	HEADER 1x3			CONN-1X3	TSW-103-07-T-S	Samtec
21	2	J4,J5	HEADER 12x2			CONN2X12-2MM	TMM-112-01-T-D	Samtec
22	1	J809	5X2 Shrouded Header			CONN2X5-4W	2510-6002UB	3M
23	1	J815	26-60-5080			CONN8NP0.156RA	26-60-5080	MOLEX

Table 3. Si3482 Smart PSE-24 Bill of Materials (Continued)

Item	Qty	Ref	Value	Rating	Tol	PCB Footprint	Mfr Part #	Mfr
24	1	J816	HEADER 8x2			CONN2X8	TSW-108-07-S-D	Samtec
25	1	J817	HEADER 5x2			CONN2X5	TSW-105-07-T-D	Samtec
26	1	L151	33 µH	0.4 A	±20%	IND-LPS4018	LPS4018-333ML	Coilcraft
27	1	Q1	MMBT3904	200 mA		SOT23-BEC	MMBT3904	Fairchild
28	2	R1,R835	0 Ω	1 A		R0603	CR0603-10W-000	Venkel
29	2	R2,R157	10 kΩ	1/10 W	±5%	R0603	CR0603-10W-103J	Venkel
30	4	R14,R804, R805,R830	1 kΩ	1/10 W	±1%	R0603	CR0603-10W-1001F	Venkel
31	30	R15,R108,R109, R110,R111,R208, R209,R210,R211, R308,R309,R310, R311,R408,R409, R410,R411,R508, R509,R510,R511, R608,R609,R610, R611,R802,R832, R838,R839,R840	10 kΩ	1/10 W	±1%	R0603	CR0603-10W-1002F	Venkel
32	6	R126,R226,R326, R426,R526,R626	44.2 kΩ	1/10 W	±1%	R0603	CR0603-10W-4422F	Venkel
33	1	R150	5.6 Ω	1/4 W	±5%	R1210	CR1210-4W-5R6J	Venkel
34	1	R151	25.5 kΩ	1/16 W	±1%	R0603	CR0603-16W-2552F	Venkel
35	1	R153	30.1 kΩ	1/16 W	±1%	R0603	CR0603-16W-3012F	Venkel
36	1	R155	2.87 kΩ	1/16 W	±1%	R0603	CR0603-16W-2871F	Venkel
37	1	R156	4.87 kΩ	1/16 W	±1%	R0603	CR0603-16W-4871F	Venkel
38	2	R833,R836	267 Ω	1/10 W	±1%	R0603	CR0603-10W-2670F	Venkel
39	2	R834,R837	2.1 Ω	1/16 W	±1%	R0603	CR0603-16W-2101F	Venkel
40	1	R841	332 Ω	1/10 W	±1%	R0603	CR0603-10W-3320F	Venkel
41	1	SW1	SW Pushbutton	50 mA		SW4N6.5X4.5-PB	101-0161-EV	Mountain Switch
42	13	TPV100,TPV200, TPV300,TPV400, TPV500,TPV600, TPV802,TPV803, TPV804,TPV805, TPV806,TPV807, TPV808	TPV			VIA-TP	N/A	N/A
43	1	TPV50x1	EPAD			VIA-EPAD	N/A	N/A
44	1	TP17	RED			Testpoint	151-207-RC	Kobiconn
45	1	TP18	WHITE			Testpoint	151-201-RC	Kobiconn
46	2	TP803,TP804	BLACK			Testpoint	151-203-RC	Kobiconn
47	1	U1	Si8423	2500 V_{RMS}		SO8N6.0P1.27	Si8423AD-B-IS-1	SiLabs
48	1	U2	Si8431	2500 V_{RMS}		SO16N10.3P1.27	Si8431BB-C-IS	SiLabs
49	6	U100,U200,U300, U400,U500,U600	Si3452			QFN40N6X6P0.5	Si3452-A00-GM	SiLabs
50	1	U152	Si3500			QFN20N5X5P0.8	Si3500-A-GM	SiLabs
51	1	U801	TLV431			TLV431-DBZ	TLV431BCDBZR	TI
52	1	U802	Si3482			QFN20N4X4P0.5	Si3482	SiLabs

4.4. Silkscreens

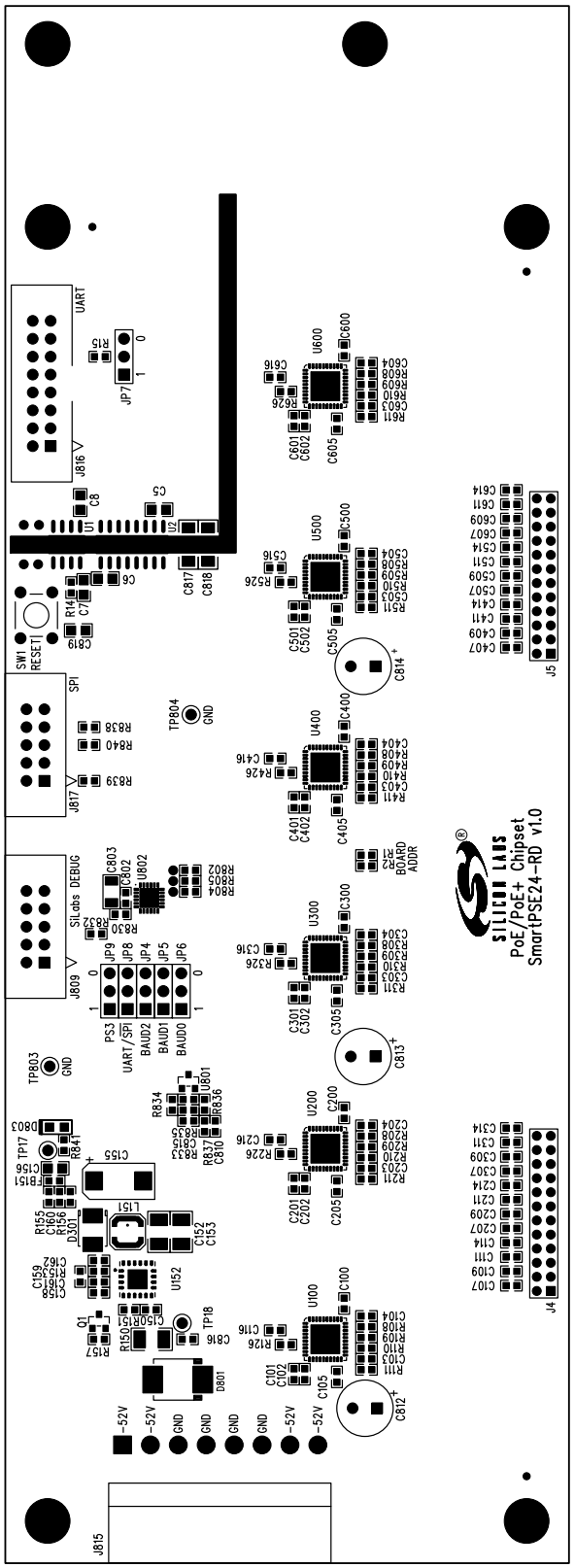


Figure 15. Smart PSE 24Silk Screen

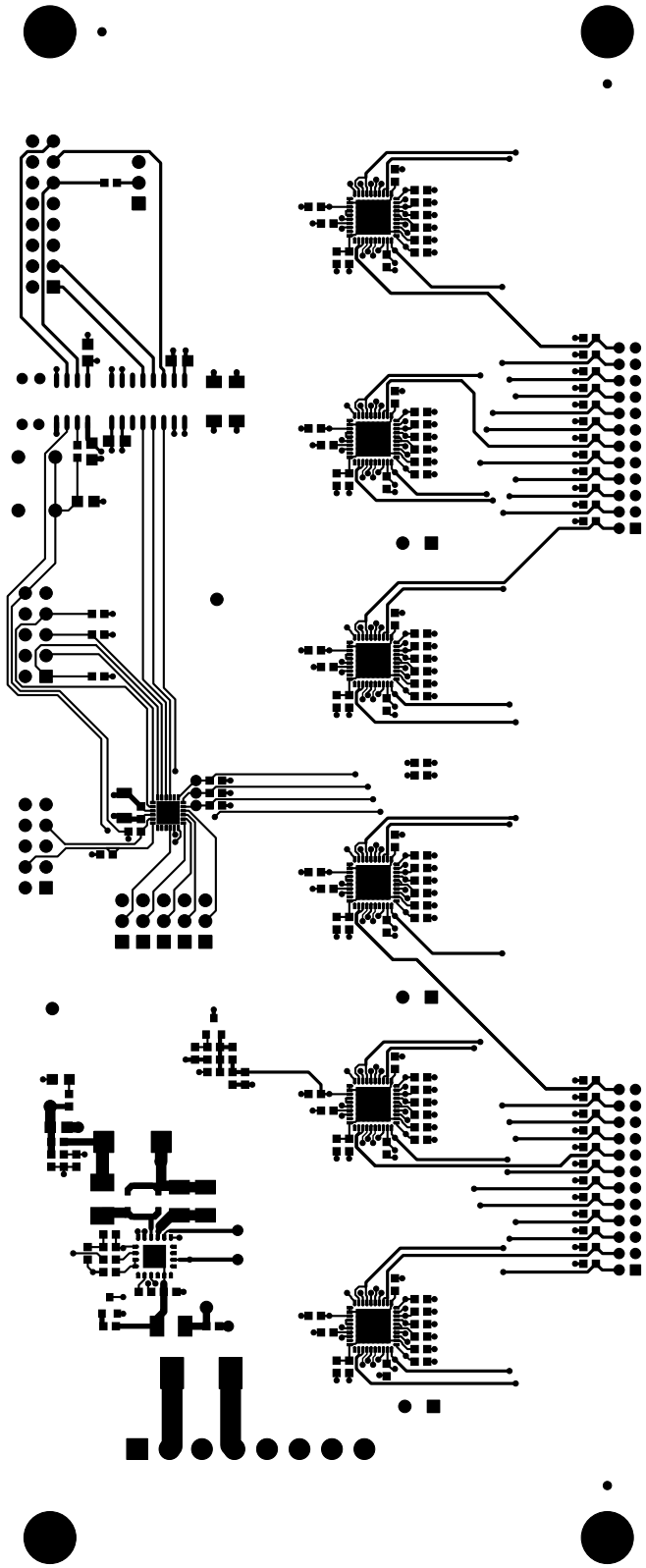


Figure 16. Smart PSE 24 Top Layer

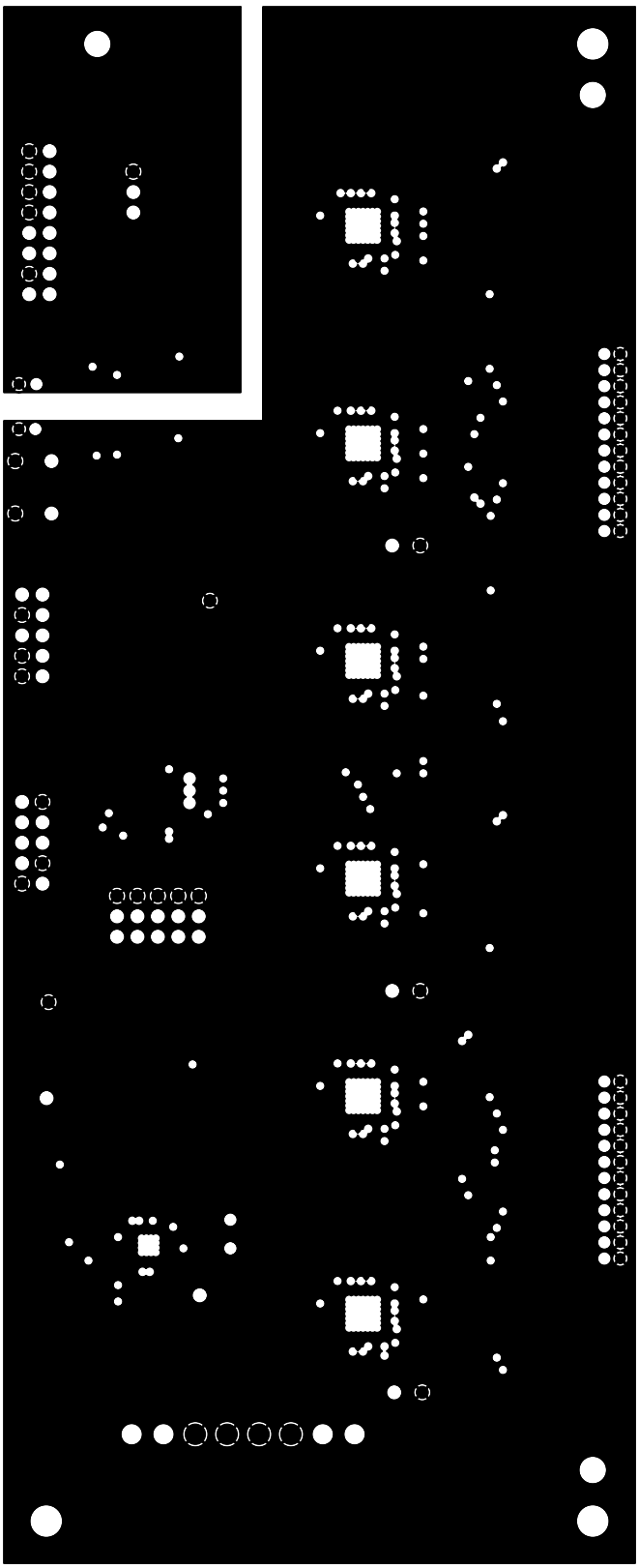


Figure 17. Smart PSE 24 Ground Layer

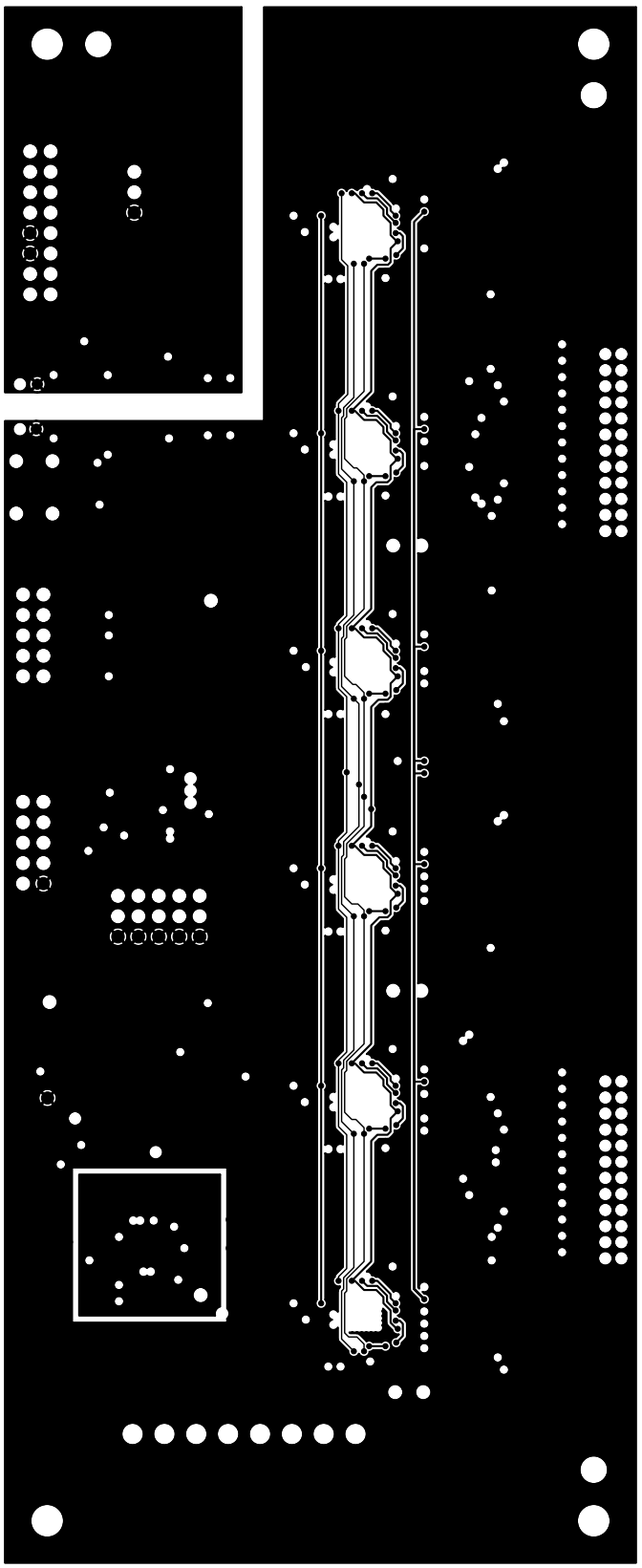


Figure 18. Smart PSE 24 Power Plane

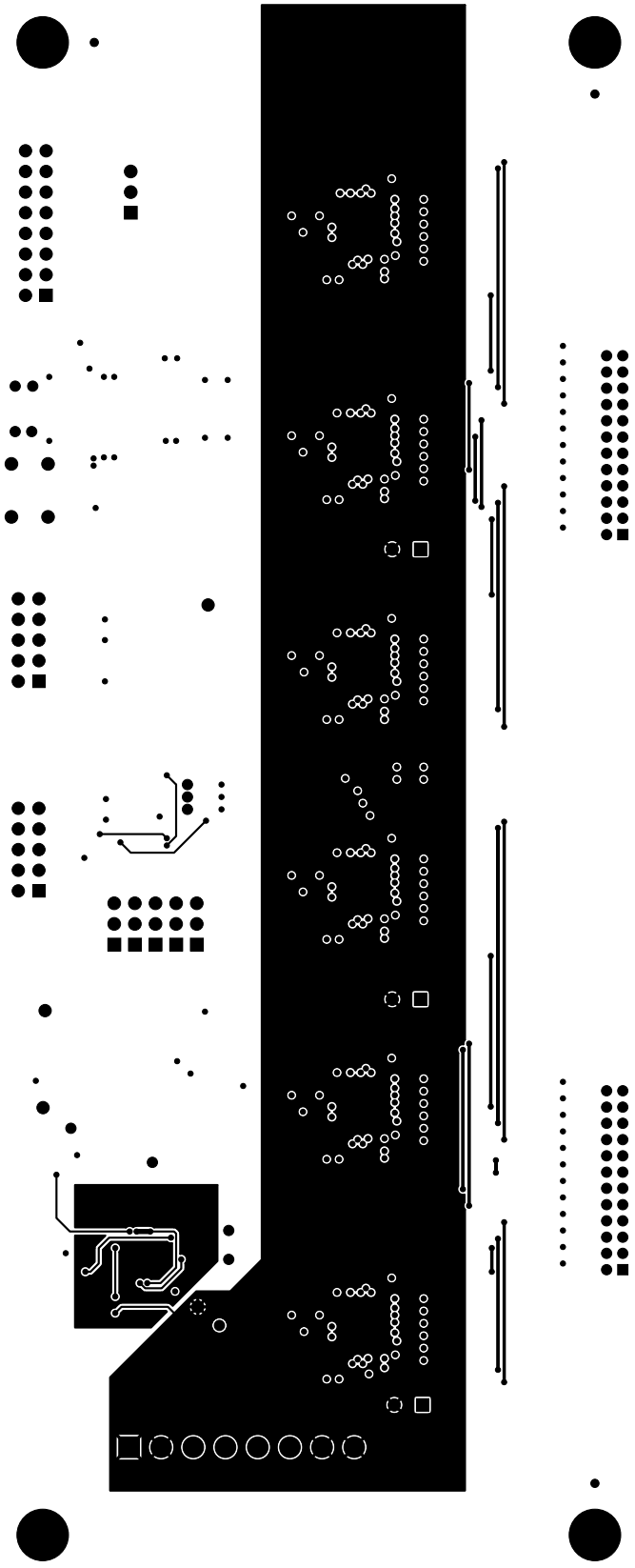


Figure 19. Smart PSE 24 Secondary Side

DOCUMENT CHANGE LIST

Revision 0.1 to Revision 0.2

- Added "Easing Software Development with the Serial Packet Protocol SDK," on page 7 to describe availability of the Serial Packet Protocol SDK.

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